UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,847	11/13/2003	Hiroyuki Higuchi	826.1903	4881

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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
DOAN, NGHIA M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/705,847	HIGUCHI, HIROYUKI
	Examiner	Art Unit
	Nghia M. Doan	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>13 November 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-16</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-2, 9-13, and 15-16</u> is/are rejected.

7)☒ Claim(s) <u>3-8 and 14</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>13 November 2003</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some *   c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>11/13/2003</u> ᴺᴹᴰ

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Responsive to communication application10/705,847 filed on 11/13/2003, claims

1-16 are pending.

Drawings

2.   The drawings are objected to because Figure 4, step 14, changes "conferting" to

"converting".   Corrected drawing sheets in compliance with 37 CFR 1.121(d) are

required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the

immediate prior version of the sheet, even if only one figure is being amended. The

figure or figure number of an amended drawing should not be labeled as "amended." If

a drawing figure is to be canceled, the appropriate figure must be removed from the

replacement sheet, and where necessary, the remaining figures must be renumbered

and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. Each drawing sheet submitted after the filing date

of an application must be labeled in the top margin as either "Replacement Sheet" or

"New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in

the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3.   Claim 16 is objected to under 37 CFR 1.75 as being a substantial duplicate of

claim 13, because the words "unit" and means for" are substantially the same. When

two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

4.   Claims 2-5, 7, 9, 11, and 14 are objected to because of the following informalities:

As claim 2, line 4, before "multi-cycle path" changes "a" to "**the**".

As claims 3 and 14, change "a signal which **can be** converted" to "**the** signal which **is** converted ".

As claim 4, line 5, changes "a memory element **can** possibly" to "**the** memory element is **possibly**".

As claim 5, states "if all of paths.... **the path are inactive for a path** which is determined not to be a multi-cycle path". It contains grammatically in this limitation. Examiner could not understand what is mean? It needs to clarify.

As claim 7, line 5, before "memory element" changes "a" to "**the**".

As claim 7, line 6, before "enable signal" changes "**an**" to "**the**".

As claim 9, Examiner suggests the claim is depending on claim 1. Therefore, claim 9, line 2, before "wherein" inserts "according to claim 1".

As claim 11, lines 4, contains " **can move is detected**", what is mean? It needs to clarify or revised.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5.   Claims 1-2, 9-13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanimoto (US 6,658,635).

6.   **With respect to claim 1**, Tanimoto discloses a multi-cycle path analyzing method (Abstract and figure 35) making an analysis of a multi-cycle path (orientation graph (V1, A1) having a side of apexes V1={CLK1, FF1, G4} and A1={((CLK1, FF1), (FF1, G4)}) which can take two cycles or more for a signal to propagate from a starting point of the path (CLK1) to its end point (FF6 {cp}) among paths within a circuit to be analyzed (figure 35, col. 27, ll. 12-17), comprising:

making an analysis of a circuit to be analyzed in correspondence with a name of each element which includes a cell configuring the circuit to be analyzed, and/or a meaning and/or a relationship of a signal to a terminal of each element (all the elements FF1, FF2, Ff3, FF4, FF5, and FF6 are flip-flops; G1, G2, G3, and G4 are logic element; and relationship of a signals, such as V1, A1, V2, A2, ...etc.) (figure 35, col. 27, ll. 7-39); and

making a multi-cycle path determination of whether or not a path from a starting point to an end point is a multi-cycle path by using a result of the analysis (col. 6, ll. 14-27, col. 12, ll. 16-20, col. 16, ll. 35-44, and col. 28, ll. 29-43).

7.   **With respect to claim 2**, Tanimoto discloses the multi-cycle path analyzing method according to claim 1, wherein: in the analysis of the circuit to be analyzed, circuit conversion (figures 27 and 35, specifically as figure 35, the first set (CLK1, FF1, G1, G2{a1}) and the second set (FF2{cp}, G4, FF3 and G3)) for a multi-cycle path analysis in correspondence with the meaning of the signal to the terminal of each element is performed (figure 35, col. 27, ll. 7-39); and the multi-cycle path determination is made by using a result of the circuit conversion (col. 28, ll. 29-43).

8.   **With respect to claim 9**, Tanimoto discloses the multi-cycle path analyzing method according to claim 1, wherein: in the analysis of the circuit to be analyzed, memory elements (flip-flop FF1-FF6) within the circuit are classified into groups (table set) by the name of each element (col. 22, ll. 43-67 and col. 23, ll. 1-42); a reachable state of a finite state machine (oriental graph) represented by each of the groups is calculated (col. 27, ll. 7-59); and the multi-cycle path determination is made by using a result of the calculation (col. 28, ll. 9-43).

9.   **With respect to claim 10**, Tanimoto discloses the multi-cycle path analyzing method according to claim 1, wherein in the analysis of the circuit to be analyzed, a restriction circuit (col. 9, ll. 60-64) corresponding to a condition is added to the circuit (figure 39, col. 18, ll. 58-64) to be analyzed based on the condition for a relationship between a value setting signal (SET/RESET) for an external input terminal of the circuit and a value read signal from an external output terminal (figure 39, col. 18, ll. 29-37, ll. 58-64); and the multi-cycle path determination is made for the circuit to be analyzed after the addition (col. 18, ll. 65-67 and col.19, ll. 1-39).

10.   **With respect to claim 11**, Tanimoto discloses the multi-cycle path analyzing

method according to claim 1, wherein a multi-cycle path restriction (col. 9, ll. 60-64)

which straddles a memory element and can move is detected by making the multi-cycle

path analysis for a path which straddles the memory element (figure 14 and 15, see the

description).

11.   **With respect to claim 12**, Tanimoto discloses the multi-cycle path analyzing

method according to claim 1, wherein: in the analysis of the circuit to be analyzed,

information required for circuit conversion for the multi-cycle path analysis is stored in

correspondence with the meaning of the signal to the terminal of each element which

includes a cell configuring the circuit (col. 28, ll. 29-43); and the multi-cycle path

determination is made by using stored contents (figure 1, element [2] and col. 28, ll. 29-

43) .

12.   **With respect to claims 13, 15, and 16**, Tanimoto discloses a multi-cycle path

analyzing apparatus (Abstract and figures 1-5) and a program which is used by

computer (Abstract) making an analysis of a multi-cycle path (orientation graph (V1, A1)

having a side of apexes V1={CLK1, FF1, G4} and A1={(CLK1, FF1), (FF1, G4)}) which

can take two cycles or more for a signal to propagate from a starting point of the path

(CLK1) to its end point (FF6 {cp}) among paths within a circuit to be analyzed (figure 35,

col. 27, ll. 12-17), comprising:

circuit converting means for (unit) (figure 1, element [1]; also see figures 2 and 3)

performing circuit conversion (figures 27 and 35, specifically as figure 35, the first set

(CLK1, FF1, G1, G2{a1}) and the second set (FF2{cp}, G4, FF3 and G3)) for making a

multi-cycle path analysis in correspondence with a meaning of a signal to a terminal of each element which includes a cell configuring the circuit (figure 35, col. 27, ll. 7-39); and

multi-cycle path determining means for (unit) (figure 1, element [11]; also see figures 4 and 5) making a determination of a path from a starting point to an end point is a multi-cycle path by using a result of the circuit conversion (col. 6, ll. 14-27, col. 12, ll. 16-20, col. 16, ll. 35-44, and col. 28, ll. 29-43).

Allowable Subject Matter

13.   Claims 3-8 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14.   The following is a statement of reasons for the indication of allowable subject matter: (as claims 3 and 14) wherein in the circuit conversion, circuit conversion such that the signal to terminal of each element which is converted into an enable signal to memory elements at the starting point and the end point of the path among signals to the terminal of the element is performed.

15.   Claims 4-8 are depending on claim 3. Therefore, claims 4-8 are also objected.

Conclusion

16.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nadcau-Dostic et al. (US 6,763,489) applying a multi-cycle signal into a test circuit for performed circuit simulating. Landman et al (US 5,191,541)

converting a multi-cycle path into a single cycle path by inserting a path break within the multi-cycle path.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

VUTHE SIEK
PRIMARY EXAMINER